

CLAIMS

What is claimed is:

- 1 1. An integrated circuit card for a test head, the integrated circuit card
2 comprising:
3 an I/O channel with an elastomeric connector;
4 pin electronics integrated circuit (PEIC) coupled to the I/O channel;
5 micromachine relays coupled to the PEIC;
6 spring pins coupled to and controlled by the micromachine relays, the
7 spring pins designed to be movably coupled to a device under test
8 (DUT);
9 a heat sink structure integral to the integrated circuit card to flow a chilled
10 substance through the heat sink structure to cool the PEICs.

1 2. The integrated circuit card of claim 1, wherein the chilled substance
2 comprises a gas or a liquid.

1 3. The integrated circuit card of claim 1, wherein the heat sink
2 structure comprises cooling channels within the integrated circuit
3 card.

1 4. The integrated circuit card of claim 1, wherein the cooling channels
2 are etched, drilled, cast, or micromachined within the integrated
3 circuit card.

- 1 5. The integrated circuit card of claim 1, further comprising a driver
2 circuit for driving a movement of the micromachine relay.
- 1 6. The integrated circuit card of claim 1, wherein the integrated circuit
2 card further includes a timing generator for generating clocking
3 and timing signals for the PEIC.
- 1 7. The integrated circuit card 6, wherein the timing generator is
2 located on the test head, thereby reducing signal delays.
- 1 8. The integrated circuit card of claim 1, further comprising a tester
2 for generating the signals used to test the DUT.
- 1 9. The integrated circuit card of claim 8, further comprising a logic
2 circuit receiving signals from the tester.
- 1 10. The integrated circuit card of claim 9, wherein the logic circuit is
2 located on the test head.
- 1 11. The integrated circuit card of claim 9, wherein the logic circuit is a
2 field programmable gate array (FPGA).
- 1 12. A testing unit comprising:
2 a computing system;

3 a test head coupled to the computing system and receiving control signals
4 from the computing system, the test head having a place for a
5 device under test (DUT), the test head comprising:
6 a location to place a DUT;
7 a plurality of spring pins for connecting signals to the DUT;
8 a plurality of micromachine relays for controlling the
9 plurality of spring pins; and
10 an integrated circuit device for controlling the relays;
11 wherein the micromachine relays are included within a
12 substrate of the integrated circuit device.

1 13. The testing unit of claim 12, wherein the test head is moveable with
2 respect to the computing system.

1 14. The testing unit of claim 12, wherein the test head is coupled to the
2 computing system via a flexible transmission line.

1 15. The testing unit of claim 14, wherein the flexible transmission line
2 is a flexible low impedance bus.

1 16. The testing unit of claim 12, wherein the testing unit further
2 includes a timing generator for generating clocking and timing
3 signals for the integrated circuit device.

- 1 17. The testing unit of claim 16, wherein the timing generator is located
2 on the test head, thereby reducing signal delays.
- 1 18. The testing unit of claim 12, further comprising a tester for
2 generating the signals used to test the DUT.
- 1 19. The testing unit of claim 18, further comprising a logic circuit
2 receiving signals from the tester.
- 1 20. The testing unit of claim 12, wherein the test head has a circular
2 body, and the integrated circuit device comprises a plurality of
3 integrated circuit cards located within the test head.
- 1 21. The testing unit of claim 20, wherein:
2 the body of the test head includes a plurality of cut-outs;
3 the integrated circuit device includes a plurality of circuit cards having
4 tops that fit within the cut-outs of the test head; and
5 the plurality of spring pins extend from the tops of the circuit cards
6 through the cut-outs.
- 1 22. The testing unit of claim 12, further comprising a micromachine
2 relay switch matrix coupled to the integrated circuit device, the
3 micromachine relay switch matrix selectively coupling signals to
4 the plurality of spring pins.

- 1 23 The testing unit of claim 22, wherein the micromachine relay switch
2 matrix comprises a plurality of switches implemented on the
3 substrate.
- 1 24. The testing unit of claim 22, wherein the micromachine relay switch
2 matrix is implemented on a hybrid circuit.
- 1 25. The testing unit of claim 12, wherein the micromachine relay
2 comprises a moveable cantilever arm controlled by electromagnetic
3 attraction/repulsion.
- 1 26. The testing unit of claim 12, wherein the micromachine relay
2 comprises rhodium contacts and a ferrite electromagnets.
- 1 27. The testing unit of claim 12, wherein the micromachine relay
2 comprises a relay built of micromachined parts.
- 1 28. The testing unit of claim 12, wherein the micromachine relay
2 comprises an electrostatic relay.
- 1 29. A tester including a moveable test head for testing a device under
2 test (DUT), the test head comprising:
3 a spring pin array designed to couple the tester to the DUT;
4 a micromachine relay array designed to control the spring pin array;

5 an integrated circuit for controlling the micromachine relay array to
6 permit testing of the DUT; and
7 a control circuitry for controlling a testing of the DUT coupled to the
8 integrated circuit.